CLAIMS

I claim:

1. A disk enclosure comprising:

a first bus coupled to a first plurality of elements powered by a first power domain;

a second bus coupled to a second plurality of elements powered by a second power domain;

a first controller coupled to a third bus; and

a first multiplexer operable to selectively couple the first or the second bus to the third bus so the first controller can communicate with the first or the second plurality of elements.

2. The disk enclosure of claim 1, wherein the first, the second, and the third buses are I2C buses.

3. The disk enclosure of claim 1, wherein the first plurality of elements includes at least one of a first temperature sensor, a first memory , and a first backplane controller.

4. The disk enclosure of claim 3, wherein the first backplane controller is coupled to a first port bypass circuit, and the first port bypass circuit operable to bypass an element in the first plurality of elements.

5. The disk enclosure of claim 4, wherein the bypassed element is a first disk drive.

6. The disk enclosure of claim 3, wherein the second plurality of elements includes at least one of a second temperature sensor, a second memory, and a second backplane controller.

7. The disk enclosure of claim 6, wherein the second backplane controller is coupled to a second port bypass circuit, the second port bypass circuit operable to bypass an element in the second plurality of elements.

8. The disk enclosure of claim 7, wherein the bypassed element is a second disk drive.

9. The disk enclosure of claim 1, further comprising:

a fourth bus coupled to a third plurality of elements powered by the first power domain;

a fifth bus coupled to a fourth plurality of elements powered by the second power domain;

a second controller coupled to a sixth bus; and

a second multiplexer operable to selectively couple the fourth or the fifth bus to the sixth bus so the second controller can communicate with the third or the fourth plurality of elements.

10. The disk enclosure of claim 9, wherein:

the first plurality of elements includes at least one of a first temperature sensor, a first memory, and a first backplane controller;

the second plurality of elements includes at least one of a second temperature sensor, a second memory, and a second backplane controller;

the third plurality of elements includes at least one of a third temperature sensor, a third memory, and a third backplane controller; and

the fourth plurality of elements includes at least one of a fourth temperature sensor, a fourth memory, and a fourth backplane controller.

11. The disk enclosure of claim 10, wherein:

the first backplane controller is coupled to a first port bypass circuit, the first port bypass circuit operable to bypass a disk drive; and

the third backplane controller is coupled to a third port bypass circuit, the third port bypass circuit operable to bypass the disk drive.

12. A disk enclosure comprising:

a first bus coupled to a first plurality of elements powered by a first power domain;

a second bus being coupled to a second plurality of elements powered by the first power domain;

a first controller coupled to a third bus;

a second controller coupled a fourth bus;

a first multiplexer operable to selectively couple the first and the third buses so the first controller can communicate with the first plurality of elements; and

a second multiplexer operable to selectively couple the second and the fourth buses so the second controller can communicate with the second plurality of elements.

13. The disk enclosure of claim 12, wherein:

the first plurality of elements includes a first backplane controller, the first backplane controller being coupled to a first port bypass circuit, the first port bypass circuit operable to bypass a first disk drive; and

the second plurality of elements includes a second backplane controller, the second backplane controller being coupled to a second port bypass circuit, the second port bypass circuit operable to bypass the first disk drive.

14. The disk enclosure of claim 13, further comprising:

a fifth bus coupled to a third plurality of elements powered by a second power domain;

a sixth bus coupled to a fourth plurality of elements powered by the second power domain;

wherein the first multiplexer is operable to selectively couple the first and the fifth buses so the first controller can communicate with the third plurality of elements; and

wherein the second multiplexer is operable to selectively couple the second and the sixth buses so the second controller can communicate with the fourth plurality of elements.

15. The disk enclosure of claim 14, wherein:

the third plurality of elements includes a third backplane controller, the third backplane controller being coupled to a third port bypass circuit, the first port bypass circuit operable to bypass a second disk drive; and

the fourth plurality of elements includes a fourth backplane controller, the fourth backplane controller being coupled to a fourth port bypass circuit, the second port bypass circuit operable to bypass the second disk drive.